

Optimization of CMOS Current Mirror Load-based Differential Amplifier using Hybrid Cuckoo Search and Particle Swarm Optimization Algorithm

Pankaj P. Prajapati*, Mihir V. Shah

Department of Electronics and Communication Engineering, L.D. College of Engineering, Gujarat Technological University (GTU), Navrangpura, Ahmedabad, Gujarat, India

Abstract

Optimization of CMOS based analog circuits is becoming a practical solution for complex analog modules. There are number of evolutionary algorithms presented to optimize the analog circuits in different reported literatures. During optimization process, the optimal result may not be obtained with only individual algorithm or requires a more time. Therefore, the hybrid algorithm of two or more algorithms is more effective method to obtain the goal. The Particle Swarm Optimization (PSO) algorithm is easy to implement and has good convergence speed. However, The Cuckoo Search (CS) algorithm has better skill to catch a global optimal result. A hybrid algorithm of CS and PSO (CSPSO) is developed to get the gains of the CS and PSO algorithms. In this work, CSPSO algorithm is tested to design the CMOS current mirror load-based differential amplifier (DA) with 180 nm CMOS technology parameters. The hybrid CSPSO algorithm is implemented with C language and interfaced with Ng-spice circuit simulator using script file. In this work, the CSPSO algorithm is used as a searching tool for transistor sizing and Ng-spice has been used as a fitness creator. The experimental simulation results show that the hybrid CSPSO algorithm outperforms with PSO and CS algorithms.

Keywords: Evolutionary algorithm, cuckoo search algorithm, particle swarm optimization algorithm, hybrid algorithm, optimization

*Author for Correspondence E-mail: pp12479@yahoo.co.in

INTRODUCTION

The most important parts of many integrated circuits design are precise design of analog circuits. The performance of an analog circuit is depending on number of design parameters so analog circuits require to optimize each design parameters. The circuit design successful depends on the circuit designer's skill. The use of optimization algorithms is increased by the analog designers as a substitute of design procedures or statistic-based procedures to design an analog circuit. Optimization is a branch of computational science which can be defined as the process of finding the best solution for a problem [1]. It is an iterative process in which value of design parameters are updated up to they achieve the optimal result. An analog circuit optimization problem concurrently depends on objective functions, different types of variables and restrictions. These type hard constrained problems are solved by meta-heuristics

algorithms [2]. There are number of metaheuristics algorithm reported in the literatures i.e. Genetic Algorithm (GA) [3], Simulated Annealing (SA) [4], Tabu Search (TS) [5], Evolutionary Programming (EP) [6], Particle Swarm Optimization (PSO) [7], Artificial Bee Colony (ABC) [8], Differential Evolution (DE) [9], Ant Colony Optimization (ACO) [10], Cuckoo Search (CS) [11], Firefly Algorithm (FA) [12], Wind Driven Algorithm (WDA) [13], Bat algorithm [14], Symbiotic Organisms Search (SOS) [15], Grey Wolf Optimizer (GWO) [16], Stochastic Fractal Search (SFS) [17], and Grass Fibrous Root Optimization Algorithm (GRA) [18].

However, each meta-heuristic has its own advantages and disadvantages. These metaheuristic algorithms generally consume considerable computing times and some parameter settings to achieve a high quality of results. Therefore, recent researchers have

tried to develop the hybrid algorithms to achieve the success.

The hybrid algorithm of CS and PSO (CSPSO) is developed using C language and used as a searching tool to optimize the CMOS current mirror load-based differential amplifier in this paper. The simulation based method is used for optimization of this circuit. The content of this paper is structured as follows. In section 2, the PSO algorithm, CS algorithm and hybrid CSPSO algorithm are concisely discussed. In section 3, the CMOS current mirror load based differential amplifier is concisely discussed. The experimental setup of this work is explained in section 4. Simulation results and discussion are explained in section 5. Conclusions are discussed in section 6.

A BRIEF OVERVIEW OF THE PSO, CS AND HYBRID CSPSO ALGORITHMS

PSO Algorithm

The PSO algorithm is a fundamentally swarm intelligent based evolutionary algorithm developed by Kennedy and Eberhart [7]. It uses set of flying birds with different velocities to find the optimal solution. The velocities of these birds are dynamically adjusted based on their past performance, as well as their neighbor in the exploration space. In this algorithm, each solution bird in folk is known as a particle. The birds in the population change their social performance based on their movement toward the destination. This algorithm works in an iteration manner and finds the best solution. The main steps for PSO algorithm are given set of flying birds with different velocities by the flow diagram as shown in Figure 1 [19].

Suppose particle swam consists N number of particles with D dimensions. The position and velocity of j^{th} particle is characterized by $X_j = [X_{j1}, X_{j2}, \dots, X_{jD}]$ and $V_j = [V_{j1}, V_{j2}, \dots, V_{jD}]$. The velocity of j^{th} particle after each iteration is updated by the following formula [20].

$$V_{jd}^{i+1} = W * V_{jd}^i + C_1 * \text{rand}_1(\text{pbest}_{jd}^i - X_{jd}^i) + C_2 * \text{rand}_2(\text{gbest}_d^i - X_{jd}^i) \quad (1)$$

Here, the range of j is {1, 2, 3..... .N}, the range of d is {1, 2, 3....., D}, the range of i is

{1, 2, 3.... maximum iteration number}, pbest is particle's personal current best position, gbest is particle's global best position, rand_1 and rand_2 are uniform distributed random numbers between 0 and 1, C_1 and C_2 are constant known as acceleration coefficients, W is known as inertia weight which is initially chosen less than one and then reduced linearly with each iteration. W controls the influence of pervious direction of displacement.

The position of the k^{th} particle in $N \times D$ dimension of the search space can be calculated using the following formula.

$$X_{jd}^{i+1} = X_{jd}^i + V_{jd}^{i+1} \quad (2)$$

Cuckoo Search Algorithm

The CS algorithm is a population based stochastic global search algorithm developed by Xin-She Yang and Suash Deb [11]. This algorithm is motivated by the exceptional lifestyle of the cuckoo species. The main steps of the CS algorithm are given by the flow diagram in Figure 2 [19]. In this algorithm, each pattern relates to a nest and each individual element of the pattern relates to a Cuckoo egg [11]. The common process equation of the CS algorithm is represented by following equation [11].

$$X_{g+1}^i = X_g^i + \alpha \otimes \text{Lévy}(\lambda) \quad (3)$$

Here, X_g is the current solution for the i^{th} cuckoo of iteration g, X_{g+1}^i is a new solution for the i^{th} cuckoo, $\alpha > 0$ is the step size which depends on scales of the problem of interests and g represents the number of the current generation. The product $\otimes$ indicates the entry wise multiplication. Lévy (λ) is random walk using Lévy flight which is more effective in the long run as compared to random walk in PSO algorithm. Lévy (λ) is derived from a Lévy distribution with an infinite variance and infinite mean [11].

$$\text{Lévy} \sim u = g^{-\lambda} \quad (4)$$

In equation (4), steps size tracks arbitrary walk procedure through a power rule spreading by heavy tailed. The CS algorithm is a population dependent stochastic optimization procedure like to PSO and DE algorithms. However, the CS algorithm takes some sort of elitism and/or selection analogous to that taken in the

harmony search (HS) algorithm [11]. The CS algorithm has more capable randomization in contrast to DE and PSO algorithms [11]. The

CS algorithm needs fewer parameters to be tuned in contrast to DE and PSO algorithms [11].

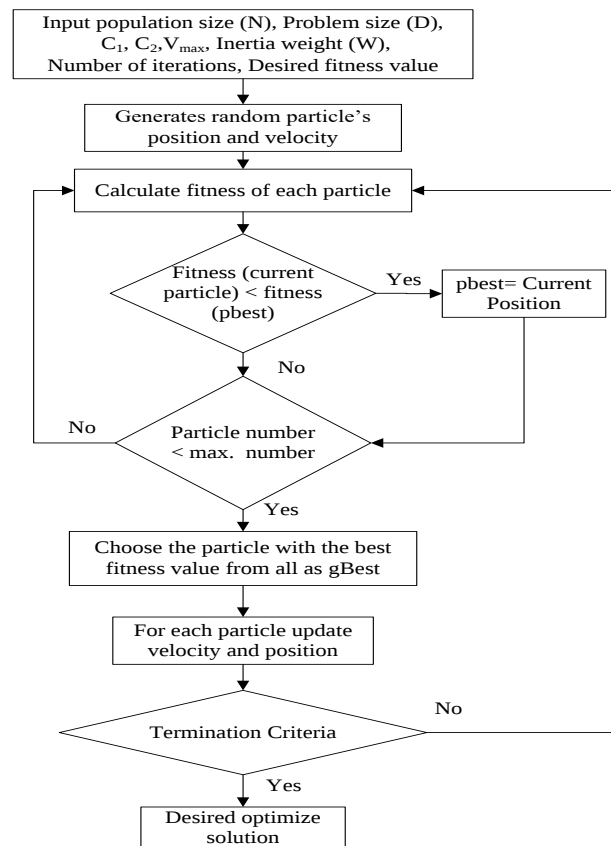


Fig. 1: Flowchart of the PSO Algorithm.

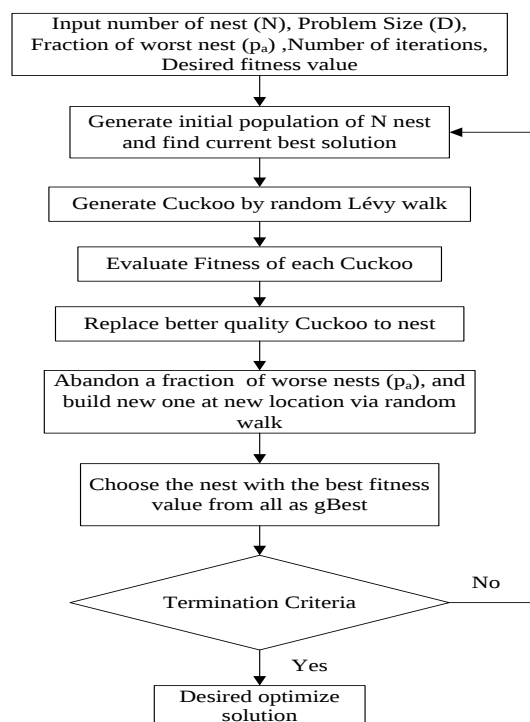


Fig. 2: Flowchart of the CS Algorithm.

Hybrid CSPSO Algorithm

The PSO is one of the most talented optimization procedure, however it converges quickly so it has premature convergence commonly in complex problems [21]. The CS algorithm may converge slightly leisurelier, but it has improved explorative talent. The CS algorithm is used to crack number of difficult problems and beat the other algorithms [22]. There is no algorithm that can powerfully optimize all optimization complications. To

resolve this problem, integration of the current algorithms can be done to find universal optimal result [23]. The convergence rate and global search ability can be improved using the hybrid algorithm [19]. It can decrease the possibility of being stuck in local minima. The hybrid algorithm can be designed to make best use of the best features of the both algorithms. The main steps of the hybrid CSPSO algorithm are given by the flow diagram in Figure 3 [19].

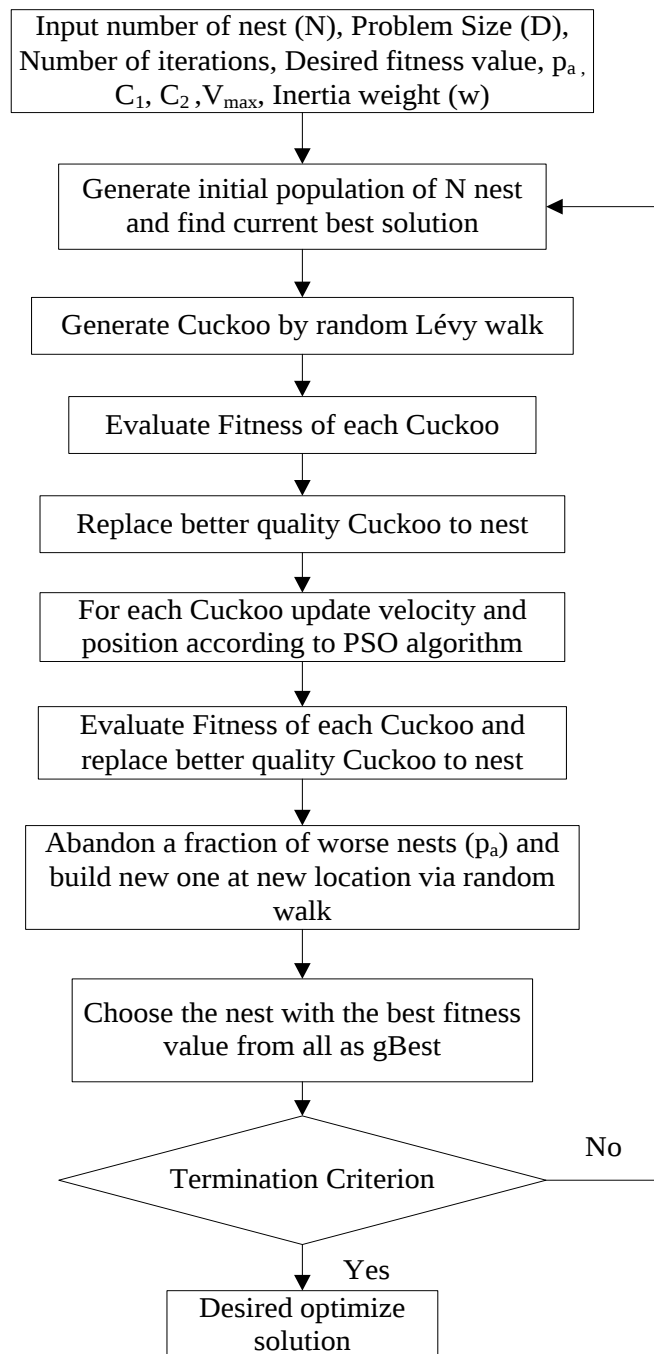


Fig. 3: Flowchart of the CSPSO Algorithm.

CMOS CURRENT MIRROR LOAD-BASED DIFFERENTIAL AMPLIFIER

The circuit diagram of CMOS differential amplifier using a current mirror load is shown in Figure 4. The main specifications of this circuit are open loop gain (A_v), unit gain bandwidth (UGB), common mode rejection ratio (CMRR), rising slew rate (RSR), falling slew rate (FSR), phase margin (PM), power dissipation (P_{diss}) and Total MOS Transistor Area (A_{MOS}) as listed in Table 1. The desired specifications for this case are nine. The main

circuit design parameters of a CMOS based analog circuit are channel width (W) and channel length (L) of different NMOS and PMOS transistors, bias current, resistor value and capacitor value. This circuit has four design parameters namely $W_1 = W_2$, $W_3 = W_4$, $W_5 = W_6$ and I_{bias} as observed from Figure 4.

So, the dimension of this optimization problem is four. More theoretical and mathematical analysis of this circuit can be found in the study Allen et al. [24].

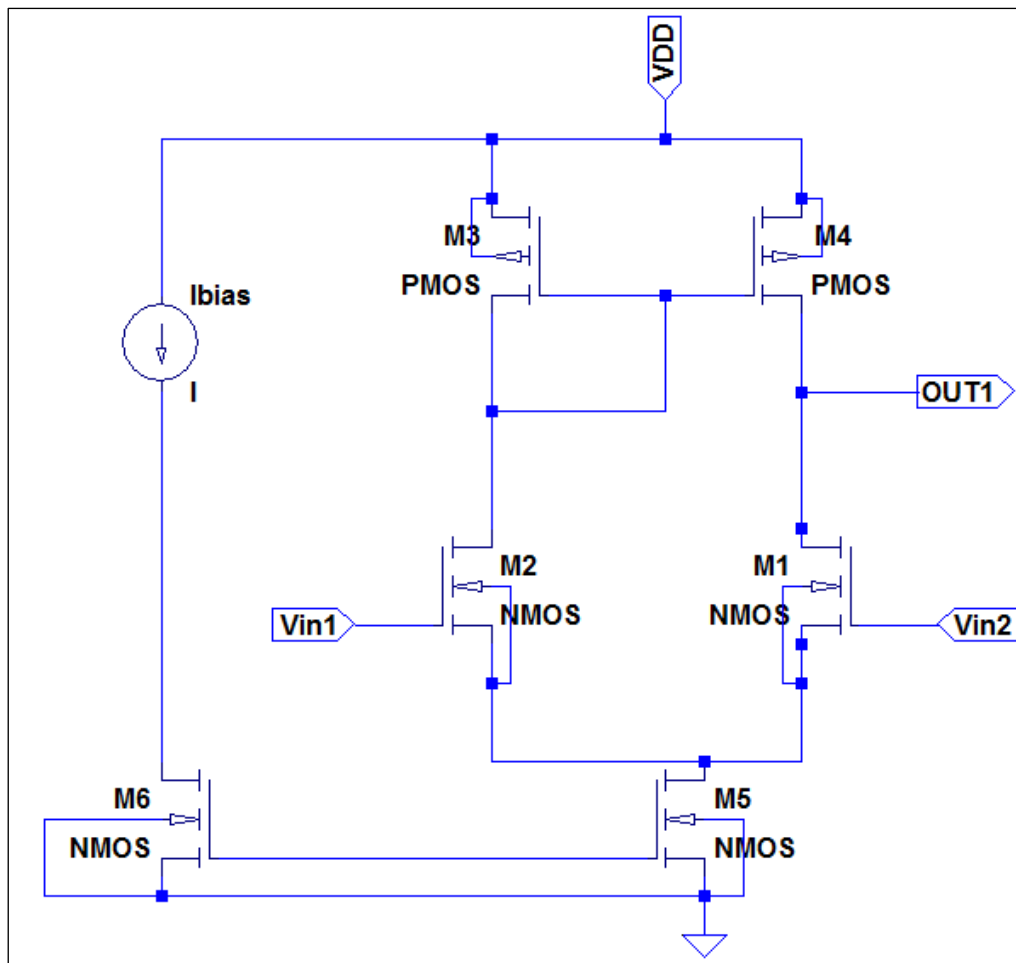


Fig. 4.: CMOS Current Mirror Load-based Differential Amplifier.

Table 1: Desired Specifications and Design Parameter Rang.

Sr. No.	Desired Specifications	Design Parameters Range
1	Output off set voltage (V_{os}) $< \pm 50$ mV	$W_1 = W_2 = 1$ to $100 \mu\text{m}$
2	$A_v > 25$ dB	$W_3 = W_4 = 1$ to $100 \mu\text{m}$
3	UGB > 10 MHz	$W_5 = W_6 = 1$ to $100 \mu\text{m}$
4	PM $> 45^\circ$	$I_{bias} = 1$ to $200 \mu\text{A}$
5	RSR > 10 V/ μs	_____
6	FSR > 10 V/ μs	_____
7	CMRR > 40 dB	_____
8	$P_{diss} < 1$ mW	_____
9	$A_{MOS} < 300 \mu\text{m}^2$	_____

EXPERIMENTAL SETUP

The optimization method for this circuit is shown in Figure 5 [25]. This method uses an optimization algorithm to generate the values of circuit design parameters and a circuit simulator to calculate circuit performance. The circuit performance is checked by the error function. This error function (F_{error}) is represented by the following formula [26].

$$F_{\text{error}} = \sum_{j=1}^M \left(\frac{\text{Specification}_{\text{Desired}} - \text{Specification}_{\text{Simulated}}}{\text{Specification}_{\text{Desired}}} \right)^2_j \quad (5)$$

Where M is the number of specifications. The RMS error proposals similar balancing to all the specifications. So, all the specifications are satisfied equally. The optimization process will halt when termination criteria will be met. then the termination criteria are maximum number of iterations or the minimum value of the error function. For this work, the minimum value of F_{error} is considered as $1e-6$. The hybrid CSPSO algorithm is developed using C language and interfaced with ngspice circuit simulator tool using script file. This experimental setup is run on a core i5, 2.4 GHz processor, 4 GB RAM with Ubuntu

12.04 operating system (OS). For hybrid CSPSO algorithm, the value of different parameters are chosen as $N = 30$, $C_1 = 1.47$, $C_2 = 1.47$, $V_{\text{max}} = 0.1X_{\text{max}}$, $V_{\text{min}} = 0.1X_{\text{min}}$, $W = [0.4, 0.9]$ and $p_a = 0.25$ [25]. Here, X_{max} is the maximum value of parameter and X_{min} is the minimum value of parameter. The maximum numbers of iterations are chosen as 100. The circuit is simulated at room temperature 27°C and supply voltage of $\pm 1.8 \text{ V}$. The experiments are repeated 10 times for this optimization problem and results are recorded.

SIMULATION RESULTS AND DISCUSSION

The obtained specifications for the differential amplifier using CMOS 180 nm technology with help of the CSPSO algorithm are listed in Table 2. The results reported of this circuit in the literatures are also listed in Table 2.

From Table 2, we can observe that the CSPSO algorithm satisfies all desired specifications for this circuit with less total MOS transistor area of $36 \mu\text{m}^2$ with compared to works reported in literatures. The optimized parameters of this circuit using the CSPSO algorithm are listed in Table 3.

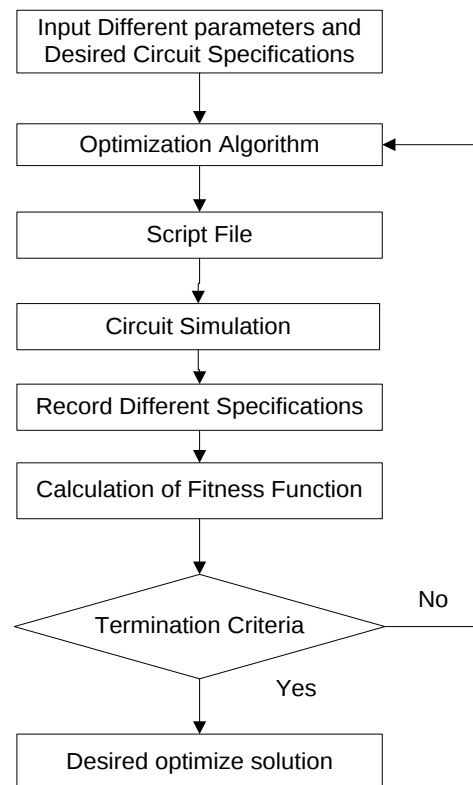


Fig. 5: Experimental Setup.

Table 2: Desired and Obtained Specifications.

Sr. No.	Desired Specifications	Obtained Specifications using the CSPSO Algorithm	Result (180 nm) [28]	Result (180 nm) [27]	Result (0.35 μm) [20]
1	$V_{os} < \pm 50 \text{ mV}$	-48.35 mV	-36.37 mV	-51.34 mV	45.91 mV
2	$A_v > 25 \text{ dB}$	26.03 dB	28.55 dB	25.66 dB	42 dB
3	$U_{GB} > 10 \text{ MHz}$	43.18 MHz	62.00 MHz	14.55 MHz	12.3 MHz
4	$PM > 45^\circ$	89.82°	90.20°	90.36°	83.8°
5	$RSR > 10 \text{ V}/\mu\text{s}$	38.78 V/ μs	49.06 V/ μs	26.08 V/ μs 25.18V/us (-ve)	— 22.4 V/us
6	$FSR > 10 \text{ V}/\mu\text{s}$	27.73 V/ μs	38.94 V/ μs	14.61 V/ μs	—
7	$CMRR > 40 \text{ dB}$	44.83 dB	46.47 dB	44.64 dB	84.2 dB
8	$P_{diss} < 1 \text{ mW}$	0.544 mW	0.408 mW	—	1.2 mW
9	$A_{MOS} < 300 \mu\text{m}^2$	36 μm^2	64.13 μm^2	54.34 μm^2	296 μm^2

Table 3: Optimized Parameters using the CSPSO Algorithm.

Sr. No.	Design Parameters Rang	Optimized Parameters using the CSPSO Algorithm
1	$W_1 = W_2 = 1 \text{ to } 100 \mu\text{m}$	21.41 μm
2	$W_3 = W_4 = 1 \text{ to } 100 \mu\text{m}$	68.95 μm
3	$W_5 = W_6 = 1 \text{ to } 100 \mu\text{m}$	33.43 μm
4	$I_{bias} = 1 \text{ to } 200 \mu\text{A}$	79.59 μA

CONCLUSIONS

In this work, hybrid algorithm of the CS and PSO is developed and tested to optimize the CMSO current mirror load based differential amplifier. The CSPSO algorithm optimizes these circuits with less transistor area as compared the PSO algorithm and DE algorithm. The hybrid CSPSO algorithm outperforms PSO and DE algorithm for optimization of CMOS differential amplifier. This hybrid approach can be tested to optimize the other CMOS based analog circuits.

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