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Optimal Cell Sizing of CMOS Two-Stage Operational Amplifier using Cuckoo Search Algorithm

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Abstract

Operational amplifier (op-amp) is commonly used in different analog circuits such as amplifiers, oscillators, comparators, digital to analog converters, analog to digital converters, mixers etc. Manual cell sizing of a CMOS based op-amp circuit for VLSI application is a challenging, boring, and time-consuming work for engineers. So, the automatic cell sizing of an op-amp is an eminent topic of growing technical and cost-effective significance. An evolutionary algorithm (EA) may be a proficient tool for automatic cell sizing of CMOS op-amp. In this study, the Cuckoo Search (CS) algorithm is demonstrated for cell sizing of CMOS op-amp with desired specifications using 0.35 and 0.18 µm CMOS technologies. The CS algorithm is developed using C language. Ngspice circuit simulator is used as a cost function producer and assessor. This optimization process is carried out in the GCC compiler on CPU Intel core™ i5-4210U@1.7 GHz processor with 4 GB RAM. Simulation outcomes show that the proposed method meets desired objectives. The simulation outcomes are also compared with previous works recorded in the literature and they show that the CS algorithm outperforms other algorithms.

Keywords: *Cell sizing, evolutionary algorithm, CS algorithm, cost function, optimization*

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INTRODUCTION

CMOS based analog circuits design is a topic of exhaustive research area for the last three decades. A differential amplifier (DA), an operational amplifier (op-amp), and operational trans-conductance amplifier (OTA) are commonly used CMOS based analog circuits in many fundamental analog blocks like filters, analog-to-digital converters (ADC), digital-to-analog converters (DAC), comparators, and mixers. So, an optimum cell sizing of these circuits is the foundation of a design setting for different uses. There are various optimization techniques reported before and in recent time for automatic cell sizing of CMOS based analog circuits. A lot of research work has been devoted to evolutionary algorithms based cell sizing of these analog circuits in different literatures. The main algorithms demonstrated for optimal cell sizing of CMOS based analog circuits in different literatures are Simulated Annealing (SA) [1], Genetic Algorithm (GA) [2, 3], Geometric Programming (GP) [4], Differential Evolution (DE) [5, 6], Particle Swarm Optimization (PSO) [7, 8], Hi-rarchical PSO (HPSO) [9], Ant Colony Optimization (ACO) [10], Harmony Search (HS) [11], and Artificial Bee Colony optimization (ABC) [12]. ABC, DE, and PSO algorithms were compared by optimizing CMOS Miller OTA by Sabat and Kumar [5]. In the study by Thakker *et al.*, low-voltage low-power analog circuits were optimized using the PSO algorithm and its modifications [9]. The performance of PSO, DE, ABC, and HS algorithms were compared by optimizing nth order filters by Vural and Ayten [13]. In the study by Pereira *et al.*, SA, GA, and PSO algorithms were demonstrated for optimal design of the LC voltage controlled oscillator (VCO) [14]. The standard PSO, ABC, and modified PSO algorithms were compared by optimizing bulk driven OTA and two stage CMOS op-amp using 130 nm CMOS technology by Patel and Thakkar [15]. Automated sizing methodology for CMOS miller OTA is demonstrated by Prajapati and Shah [16].

In this work, the Cuckoo Search (CS) algorithm is used as a searching tool for optimal sizing of

a cell for CMOS two-stage op-amp. The CS algorithm has not been tested for the cell sizing for CMOS based analog circuits beforehand. C language is used to develop the source code of the CS algorithm. The simulation-based approach is used for optimal sizing of a cell for CMOS two-stage op-amp. GCC compiler is interfaced with Ng-spice circuit simulator using script file to run this test setup. The CS algorithm is discussed in the next part of the paper. Then, CMOS two-stage op-amp is discussed, the methodology of cell sizing for CMOS two-stage op- amp using the CS algorithm is demonstrated, simulations outcomes and discussion are reported and finally, the conclusions are discussed.

CUCKOO SEARCH ALGORITHM

The CS algorithm proposed by Yang and Deb is a population-based stochastic universal search algorithm, same as DE and PSO algorithms [17]. However, this algorithm uses some type of exclusiveness and/or selection, same to that used in HS [17]. In the study by Yang and Deb, the performance of the CS algorithm was compared with the DE and PSO algorithms using some of the standard benchmark functions [17]. They concluded that the randomization is more efficient in the CS algorithm as compared to the PSO and DE algorithms [17]. Yang and Deb and Prajapati and Shah also noted that the CS algorithm requires less parameters to be adjusted as compared to the DE and PSO algorithms [17, 18]. This algorithm mimics the special lifestyle of the cuckoo species. In this algorithm, each pattern relates to a nest and each individual element of the pattern relates to a cuckoo egg. The common process of this algorithm can be given by the following equation [17]:

$$X_{t+1;\,i}=X_{t;i}+\alpha\otimes\text{Lévy}(\lambda) \quad (1)$$

Here, $X_{t;i}$ is the current solution for the ith cuckoo of iteration t, $X_{t+1;i}$ is new solution for the ith cuckoo, $\alpha>0$ is the step size which depends on scales of the problem of interests. The product $\otimes$ indicates the entry wise multiplication. Lévy (λ) is random walk using Lévy flight which is more effective in the long run as compared to a random walk in the PSO algorithm. Lévy (λ) is derived from a Lévy distribution with an infinite variance and infinite mean [17].

$$\text{Lévy}\sim u=t-\lambda \quad (2)$$

Here, $1<\lambda\leq 3$ and steps size follows random walk process with a power law distribution with heavy-tailed. The Mantegna algorithm is used to generate the Lévy walk [19]. The pseudo code of the CS algorithm is given in Algorithm 1.

Algorithm 1: CS Algorithm [17]
Begin
Objective function f (x), $x=(x_1, x_2, x_3, x_4, ..., x_d)$;

Initial a population of n host nests x_i (i=1, 2, 3, ..., n);

while (t<Max. Generation) or (stop criterion);
Get a cuckoo (say i) randomly by Lévy flights;
Evaluate its quality/fitness f_i;
Choose a nest among n (say j) randomly;
if ($f_i > f_j$) then
Replace j by the new solution;
end if
Abandon a fraction (p_a) of worse nests and build new ones at new locations;
Keep the best solutions;
Rank the solutions and find the current best;
end while
end

An analysis of all the advanced improvements for the CS algorithm comprising the discussions of theoretical background, different variants of the CS algorithm, engineering optimization applications, and research guideline for impending improvements of this influential algorithm is presented by Fister *et al*. [20]. The CS algorithm is much more efficient in finding the global optima with higher success rates [17]. The randomization is more efficient in the CS algorithm as compared to the GA and PSO algorithms as the step size is heavy tailed with any possible large step size. The CS algorithm has outperformed the GA, DE, PSO, and other meta-heuristic algorithms due to these two primary reasons [17]:

1) A fine balance of exploration and exploitation, and
2) Less number of control parameters.

The CS algorithm requires very few parameters which makes it less complex and thus

potentially more generic. The PSO algorithm is simple and has good convergence speed. On the other hand, the CS algorithm has good ability to find global optimum. The main applications of the CS algorithm reported are data clustering, data fusion, multi-level image thresholding, flood forecasting, traveling salesman problem, wireless sensor networks, flow shop scheduling, ontology matching, speaker recognition, web server composition, computer games and many more real work applications [20]. As per surveyed by us, the CS algorithm had not been used yet to optimize CMOS based two-stage op-amp. So, the CS algorithm has been tested first time for automatic sizing of CMOS two-stage op-amp in this work.

CMOS TWO-STAGE OP-AMP

Figure 1 shows the circuit diagram of CMOS two-stage op-amp. The key parts of this circuit are bias circuit, differential gain stage, and second gain stage. The manual design procedure and theory background of this circuit can be found in [8]. This circuit can be characterized by different specifications as given in Table 1. The main specifications of the two stage CMOS op-amp circuit are open loop gain, unity gain frequency, common mode rejection ratio, power supply rejection ratio, slew rate, phase margin, and power consumption. The main design parameters for this circuit are MOS transistor dimension (Width-W and Length-L), biasing current (I_{bias}), compensation capacitance (C_C), and load capacitance (C_L). The desired specifications of this circuit are governed by the circuit parameters optimized during the optimization process. The design parameters are provided within limits to obtain desired specifications.

Setup for Optimal Cell Sizing of CMOS Two-Stage Op-Amp

Figure 2 shows the basic setup for optimal cell sizing for CMOS two-stage op-amp.

This setup consists of an optimization algorithm and a circuit simulator to size CMOS two-stage op-amp for desired specifications. The script file is written to provide proper synchronization between the circuit simulator and the optimization algorithm. Initially, desired specifications of CMOS two-stage op-amp are decided. Then, the different design parameters are randomly created using optimization algorithm within their upper and lower range. The design parameters generated by the optimization algorithm are given to the circuit simulator to produce simulation results. Based on simulation results produced by the circuit simulator, the fitness function for a particular circuit is calculated. Next step is to check the termination criteria. If termination criteria are met, then the optimization procedure will terminate. If termination criteria are not met, then a new set of design parameters will be generated by the optimization algorithm based on the fitness function result. The termination criteria are a minimum value of the fitness function or a maximum number of repetitions. The main job of the optimizer is to decrease the value of fitness function for the given circuit. The value of objective function is evaluated using following equation:

$$f(x) = \sum_{j=1}^{D} \left(\frac{Spec_{Desired} - Spec_{Simulated}}{Spec_{Desired}} \right)_j^2 \quad (3)$$

Here, D is the number of specifications. The RMS error offers the same weighting to all the specifications. So, the optimizer tries to obtain all the specifications with equal importance. For this work, minimum value of the objective function is chosen as 1e-6 and the maximum number of repetitions is chosen as 100. In this work, the CS algorithm is used for optimal sizing of the cell for CMOS two-stage op-amp. This test setup has been run on a core i5, 2.4 GHz processor with 4 GB internal RAM using Ubuntu operating system. The source code of CS algorithm is implemented using C language and executed on the GCC compiler. All circuits are simulated using Ngspice-26.

Table 1: *Desired Specificaiton of Two-stage Op-amp.*

Sr. No.	Desired Specifications	Values
1	Output off set voltage (V_{os})	<±10 mV
2	Open loop gain (A_V)	>72 dB
3	Unit gain bandwidth (UGB)	>10 MHz
4	Phase margin (PM)	>45
5	Rising slew rate (RSR)	>10 *V/µs*
6	Falling slew rate (FSR)	>10 *V/µs*
7	Common mode rejection ratio (CMRR)	>70 dB
8	Power supply rejection ratio (PSRR) (+Ve)	>80 dB
9	PSRR (-Ve)	>80 dB
10	Power dissipation (P_{diss})	<1 mW
11	Total transistor area (TTA)	<300 μm^2

SIMULATION RESULTS AND DISCUSSION

The CS algorithm has only two control parameters. First is the population of a host (n) and second is abandon a fraction of worse nests (pa). In this work, we have taken n=30 and pa=0.25 as recommended by Yang and Deb [17]. The CS algorithm is tested for cell sizing of CMOS two-stage op-amp with desired specifications using 0.35 and 0.18 µm CMOS technologies. The circuit is optimized to drive the load capacitor (cl) of 0.5 pF. We have set length of M1, M2, M5, M7, and M8 transistors as L1=L2=L5=L7=L8=1.75 µm and length of M3, M4, and M6 transistors as L3=L4=L6=1.00 µm for 0.35 µm CMOS technology. We have set length of M1, M2, M5, M7, and M8 transistors as L1=L2=L5=L7=L8=0.75 µm and length of M3, M4, and M6 transistors as L3=L4=L6=0.50 µm for 0.18 µm CMOS technology. The value of compensation capacitance (C_C) is set to 0.9 pF. The design parameters range and optimized parameters of this circuit using 0.18 and 0.35 µm CMOS technologies by the CS algorithm are listed in Table 2. We have used supply voltage equal to ±1.8 V for 0.18 µm CMOS technology and 3.3 V for 0.35 µm CMOS technology. Temperature is set equal to 27ºC.

Figure 3 shows the simulation result of voltage transfer characteristic (VTC) for the circuit using 0.18 µm CMOS technology. This simulation is used to determine V_{os}, i.e. 0.10 mV. Figure 4 shows the simulation result of frequency response for this circuit using 0.18 µm CMOS technology. Using this simulation result, we can find A_v equal to 72.25 dB, PM equal to 57.06º and UGB equal to 13.57 MHz. Figure 5 shows the simulation result of CMRR for the circuit using 0.18 µm CMOS technology. Using this simulation result, we can determine CMRR equal to 76.52 dB. Figure 6 shows the simulation result of input/output waveform for this circuit using 0.18 µm CMOS technology. Using this simulation result, we can determine RSR equal to 11.09 V/µs and FSR equal to 10.61 V/µs. Figures 7 and 8 show the simulation results of PSRR (+ve) and PSRR (-ve) for this circuit using 0.18 µm CMOS technology. Using these simulation results, we can determine PSRR (+ve) equal to 82.12 dB and PSRR (-ve) equal to 124.31 dB.

From Table 3, obtained results can be compared with the previous works reported in literature. In this work, we have considered more desired specifications as compared to previous work reported in Vural and Yildirim [7], so that, the complexity of this optimization problem is more. This circuit designed was with 0.18 and 0.35 µm CMOS technologies and satisfied all desired specifications. This circuit design has more gain of 72.25, less total MOS transistor area of 14.12 μm^2, and low power consumption of 0.08 mW as compared to work reported for 0.18 µm CMOS technology. This circuit designed with 0.35 µm CMOS technology also obtained more gain of 74.29, less total MOS transistor area of 21.62 μm^2, and low power consumption of 0.49 mW as compared to work reported by Vural and Yildirim [7]. The average CPU time taken to size the cell of two-stage op-amp is 6608 sec for 0.18 µm CMOS technology and 3803 sec 0.18 µm CMOS technology for 10 independent runs.

CONCLUSIONS

In this study, the CS algorithm is tested first time to size the cell of two-stage CMOS op-amp circuit. The results of this work represent that this is a truthful and artistic method to size the cell of an analog circuit. The CS algorithm designed two-stage CMOS op-amp which has

Table 2: *Optimized Prameters for CMOS Two-stage Op-amp.*

Sr. No.	Design Parameters Range	Optimized Parameters (0.18 µm CMOS Technology)	Optimized Parameters (0.35 µm CMOS Technology)
1	W_1=W_2=1 to 10 µm	2.51 µm	5.41 µm
2	W_3=W_4=1 to 10 µm	2.13 µm	3.18 µm
3	W_5=W_8=1 to 10 µm	1.00 µm	1.85 µm
4	W_6=1 to 10 µm	9.90 µm	9.24 µm
5	W_7=1 to 10 µm	2.59 µm	3.9 µm
6	I_{bias}=1 to 10 µA	8.52 µA	9.97 µA

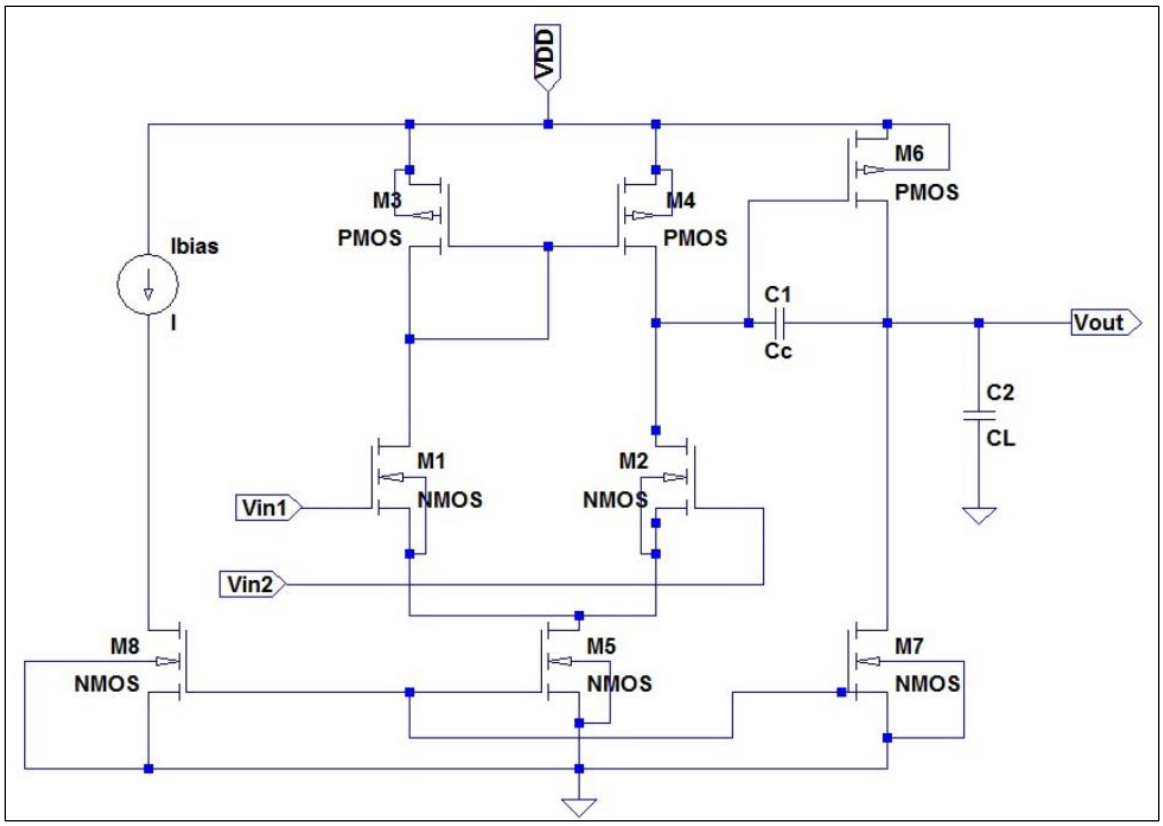

Fig. 1. *CMOS Two-stage Op-amp.*

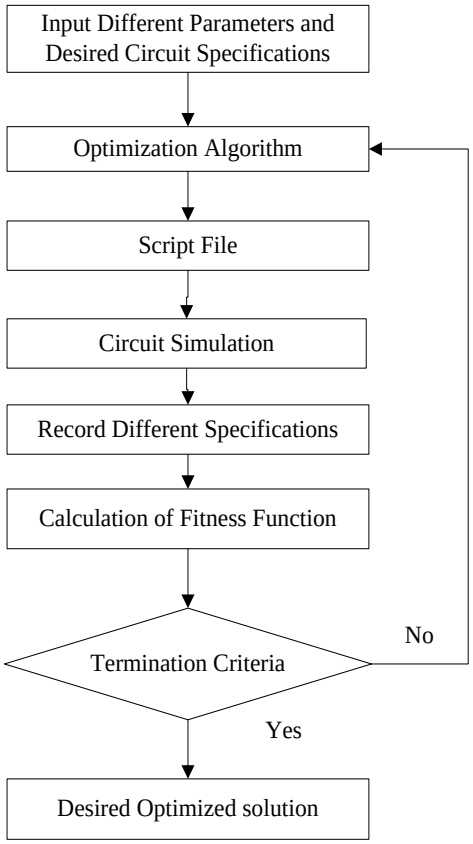

Fig. 2. *Setup for Optimal Cell Sizing of CMOS Two-stage Op-amp.*

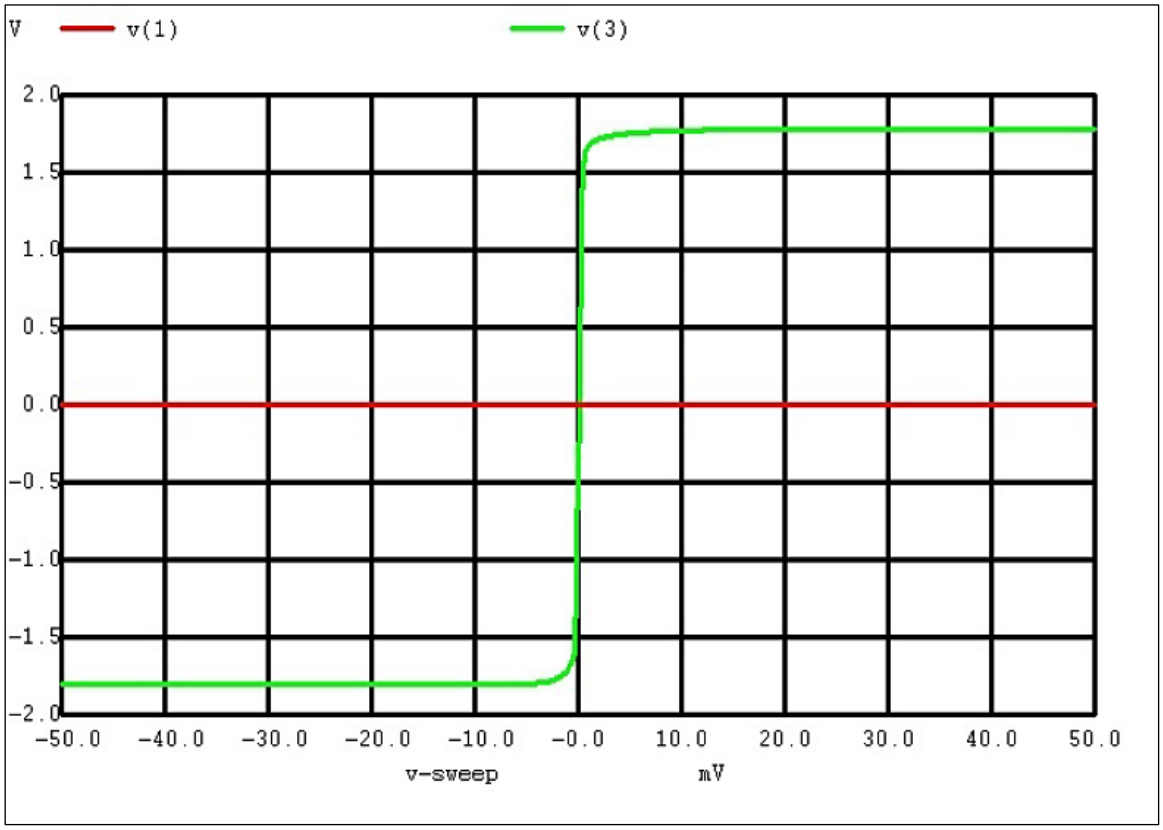

Fig. 3. *VTC of CMOS Two-stage Op-amp.*

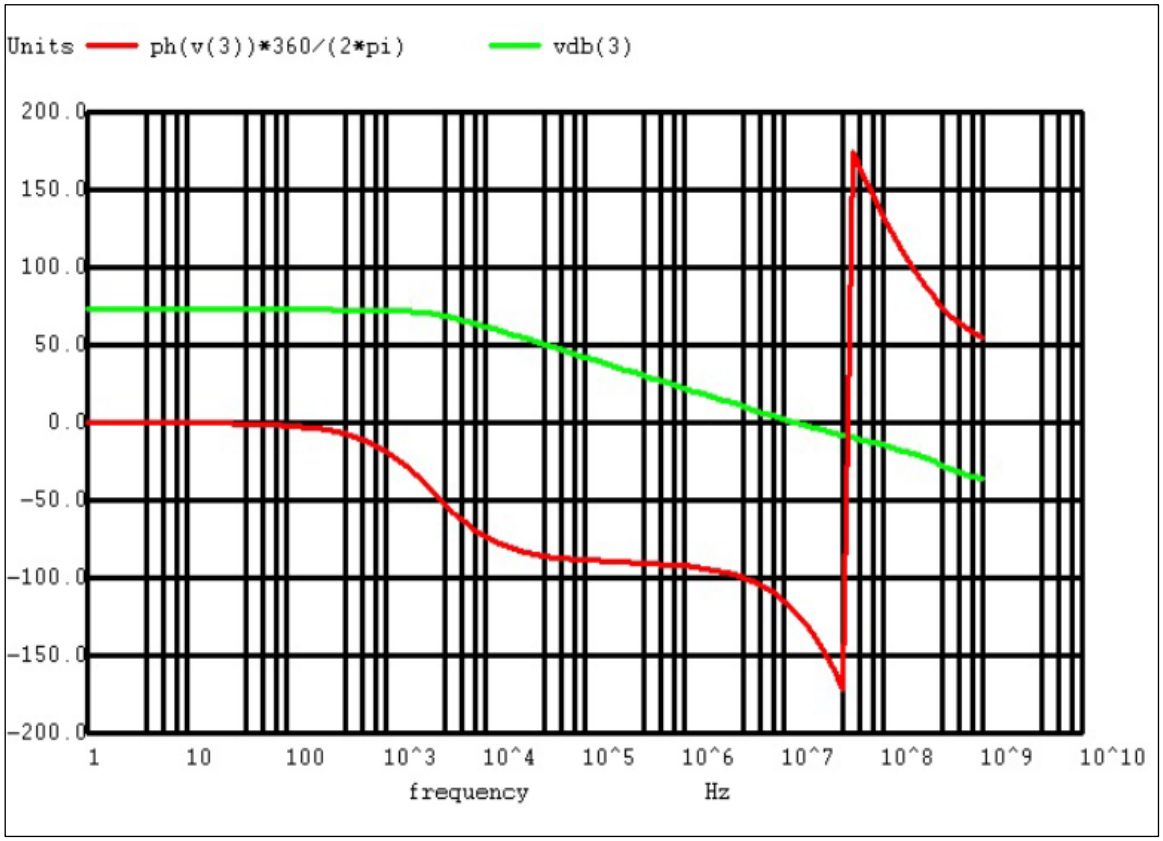

Fig. 4. *Frequency Response of CMOS Two-Stage Op-amp.*

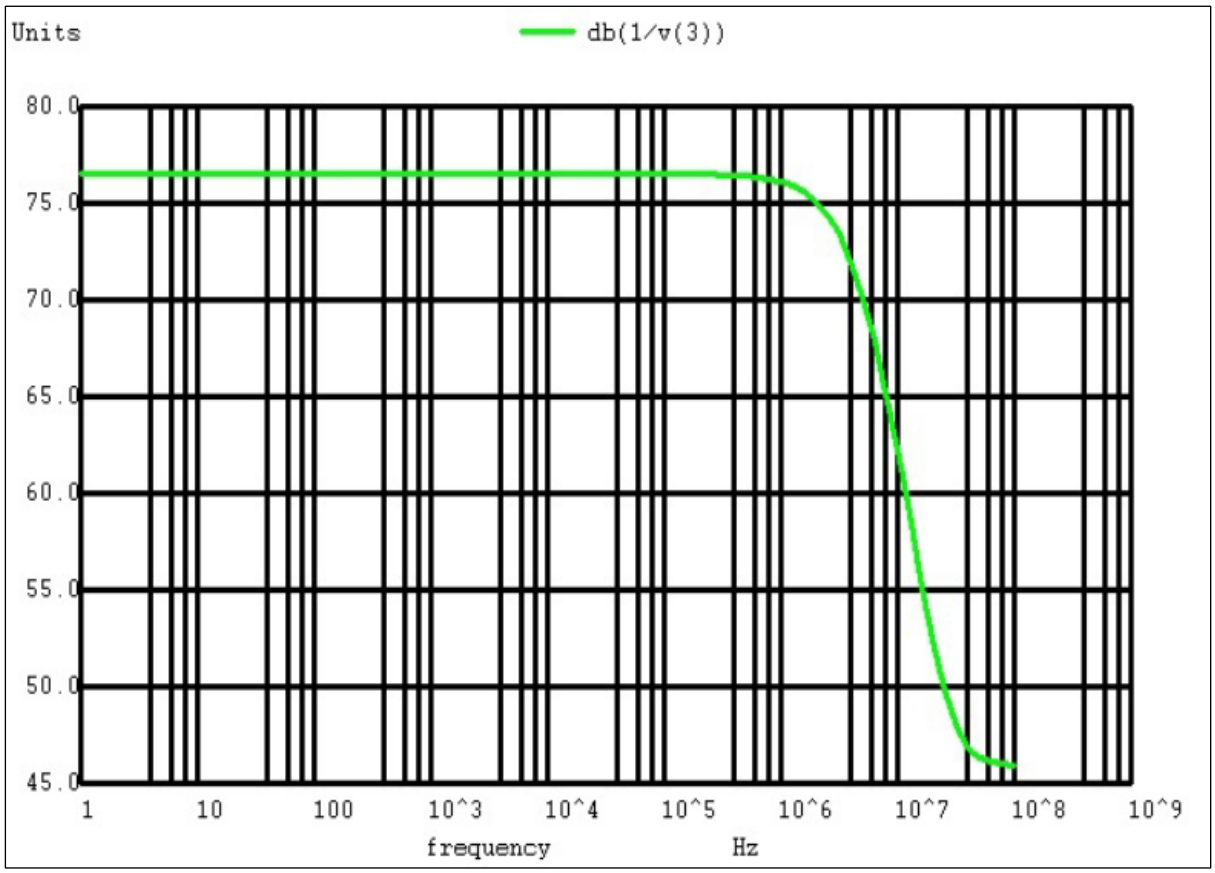

Fig. 5. *CMRR of CMOS Two-Stage Op-Amp.*

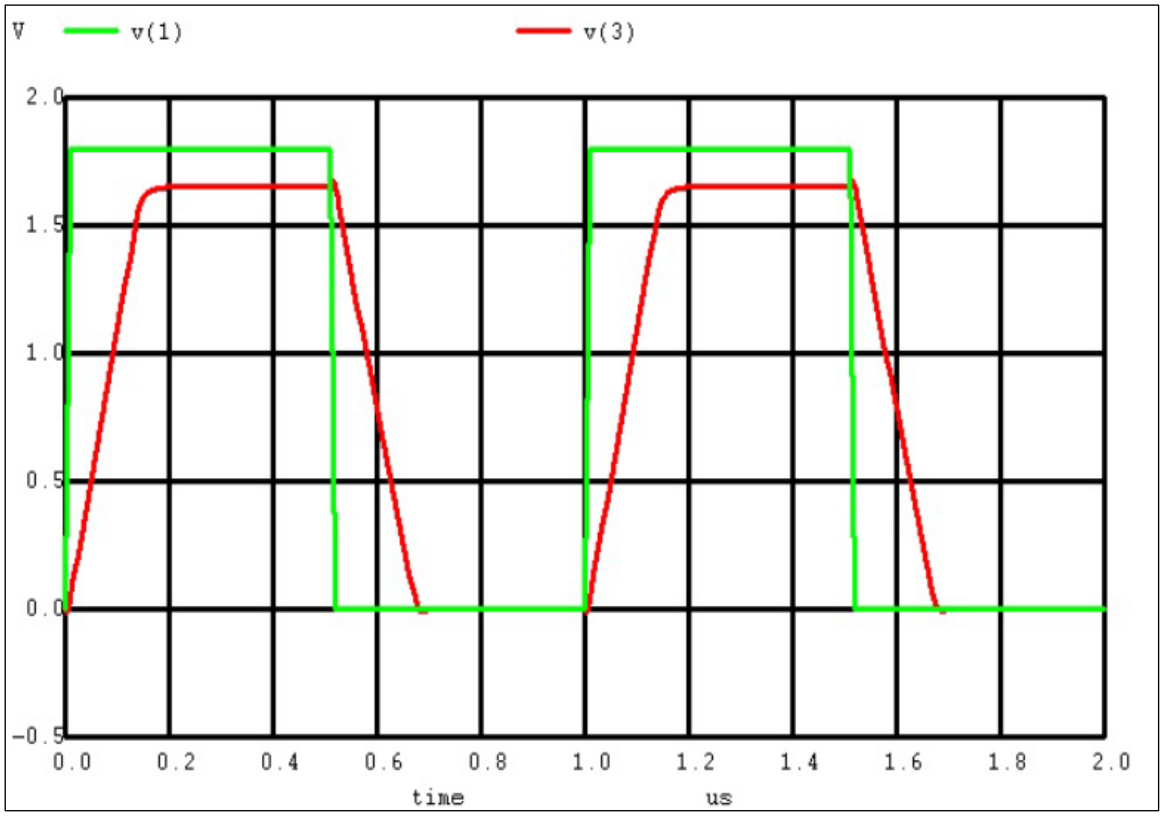

Fig. 6. *Input/Output Waveform of CMOS Two-Stage Op-Amp.*

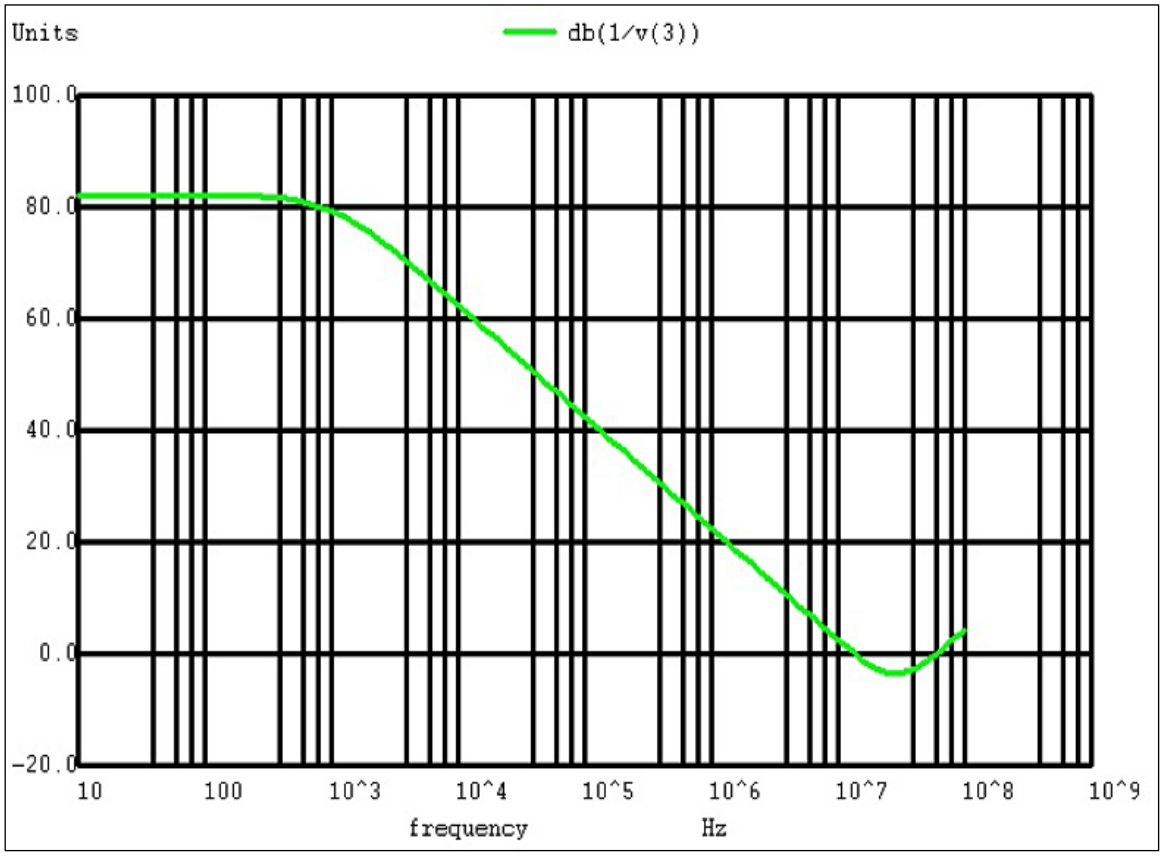

Fig. 7. *PSSR(+ve) of CMOS Two-Stage Op-Amp.*

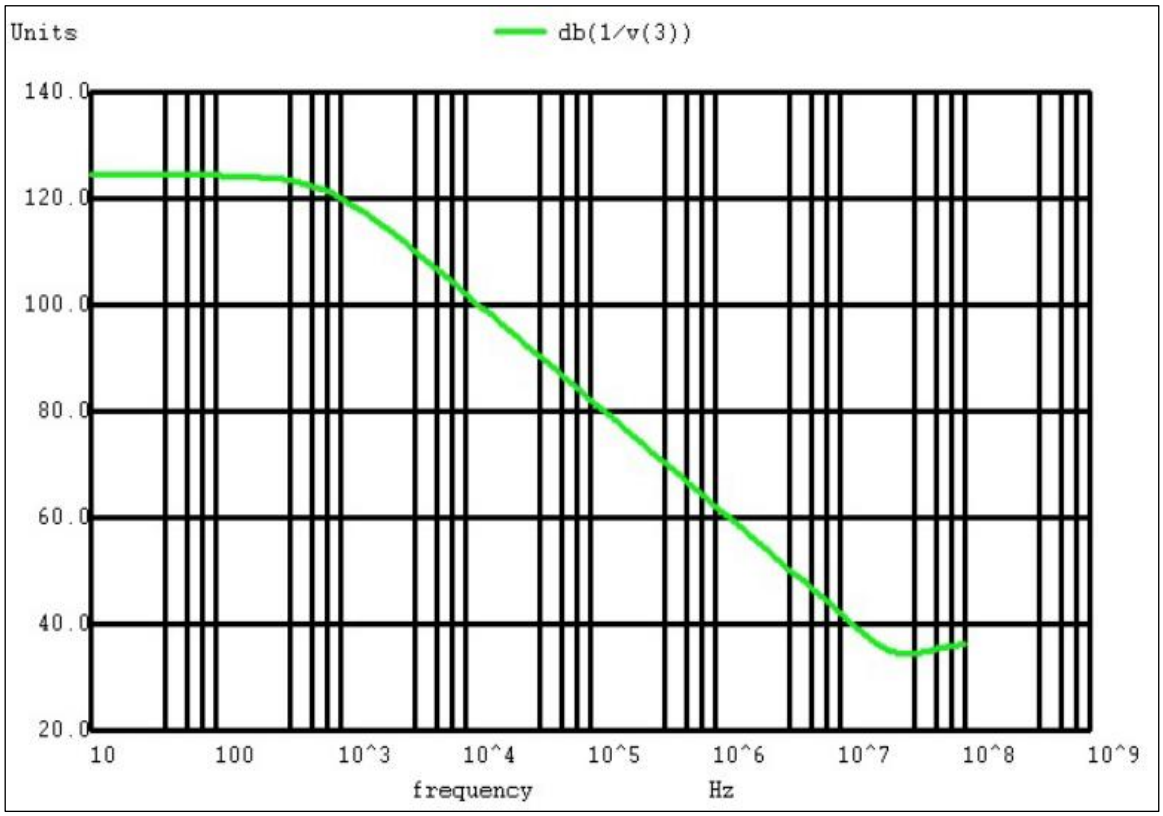

Fig. 8. *PSSR(-ve) of CMOS Two-Stage Op-Amp.*

Table 3: *Obtained Outcomes for CMOS Two-stage Op-amp.*

Sr. No.	Desired Specifications	Obtained Outcomes Using 0.18 µm	Obtained Outcomes Using 0.35 µm	[7] 0.35 µm	0.18 µm
1	V_{os} (mV)	0.10	0.48	–	–
2	A_V (dB)	72.25	74.29	63.8	65
3	UGB (MHz)	13.57	11.60	5.32	34
4	PM	57.06º	46.68º	68.3º	60º
5	RSR (V/µs)	11.09	10.52	–	20
6	FSR (V/µs)	10.61	12.92	11.13	–
7	CMRR (dB)	76.52	76.73	83.74	–
8	PSRR +Ve (dB)	82.12	90.47	78.27	–
9	PSRR -Ve (dB)	124.31	80.83	93.56	–
10	P_{diss} (mW)	0.08	0.49	2.37	0.301
11	TTA (μm^2)	14.12	21.62	265	–

more gain, less total MOS transistor area and low power consumption with fulfilled sustaining all desired specifications. This method requires less time to design an analog circuit compared to manual design. This technique can also be tested to size the cell of other CMOS based analog circuits. Process (P), Voltage (V), and Temperature (T) variations can be added with optimization process to develop robust CMOS based analog circuit design as a future work.

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